

United States Patent [19]

Agarwal et al.

US005825677A

[11] Patent Number: 5,825,677
[45] Date of Patent: Oct. 20, 1998

[54] NUMERICALLY INTENSIVE COMPUTER ACCELERATOR

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[21] Appl. No.: 619,456

[22] Filed: Mar. 20, 1996

Related U.S. Application Data

[63] Continuation of Ser. No. 217,533, Mar. 24, 1994, abandoned.

[51] Int. Cl.⁶ G06F 17/16

[52] U.S. Cl. 364/736.03

[58] Field of Search 364/736, 736.03

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[57] ABSTRACT

A matrix processing unit is described which permits high speed numerical computation. The processing unit is a vector processing unit which is formed from a plurality of processing elements. The *i*th processing unit has a set of *N* registers within which the *i*th elements or words of *N* vectors of data are stored. Each processing element has an arithmetic unit which is capable of performing arithmetic operations on the *N* elements in the set of *N* registers. Each vector of data has *K* elements. Therefore, there are *K* processing elements. A vector operation of the matrix processing unit simultaneously performs the same operation on all elements of two vectors or more. A subsequent vector operation can be performed within one machine cycle time after the preceding vector operation.

16 Claims, 5 Drawing Sheets

